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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,098	03/29/2001	Thomas D. Fletcher	42390P9006	8394

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

NV

Office Action Summary	Application No. 09/823,098	Applicant(s) FLETCHER ET AL.
	Examiner Minh Nguyen	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,18-21 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,18-21 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicants' response to the restriction requirement and amendment on 3/22/02 has been received and entered in the case. The following is a detailed Office Action of the elected claims 1-11, 18-21 and 28-30.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore,

(i) the receiver which is in a clock distribution network, and the duty cycle correction circuit which is at the receiver as recited in claim 1 (note that Fig. 7 shows the receiver 725 is outside the clock distribution network 710 and the duty cycle correction circuit 705 is in between, i.e., the receiver 725 is not in the clock distribution network),

(ii) the feedback path between the input and output of the duty cycle correction circuit (note that the path must be between the input and output of the duty cycle correction circuit),

must be shown or the features canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because it uses words which can be implied, i.e., “is provided”. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the recitation on lines 2-4 is indefinite because it is unclear whether the recitation means the clock distribution network receives the distributed clock signal or the signal which is output from the duty cycle correction circuit. It is further noted that if the clock

distribution network receives the signal which is output from the duty cycle correction circuit, the recitation is misdescriptive because the receiver is in the clock distribution network.

As per claims 2-5, these claims are rejected because of the indefiniteness of claim 1.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, 18-21 and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,008,636, issued to Markinson et al.

As per claim 1, Markinson discloses an apparatus (Fig. 2) comprising:

a duty cycle correction circuit (the circuits 112, 110, 118, 120, 122 and 124) at a receiver (the node that receives the signal outputted from the circuit VCXO 108)) in a clock distribution network 74, the duty cycle correction circuit to correct the duty cycle of a distributed clock signal (the signal at the receiver) received at the receiver.

As per claim 2, the recited feedback path reads on the path from the output of the delay line circuit 110, to the circuits 118, 120, 122, 124 and back to the duty cycle control circuit 112 to control the delay of a circuit path in the duty cycle correction circuit.

As per claim 3, the recited limitation is disclosed in column 3, lines 6-7, i.e., a symmetrical 36.36 MHz clock duty cycle.

As per claim 4, the recited frequency multiplying circuitry is disclosed in column 3, lines 54-62, i.e., receives the clock signal having the frequency 18.18 MHz and generates the clock signal having the frequency 36.36 MHz.

As per claim 5, the recited smart buffer reads on the bus interface shown in Fig. 1, in the block circuit 70A, i.e., the bus interface is used to ensure the proper operation of the duty cycle correction circuit over a range of loads (carried on the X-BUS) to be coupled to the duty cycle correction circuit.

As per claim 6, Markinson discloses a clock distribution network (Fig. 1) comprising:

clock generation circuitry 54 at a first location (the location which houses the clock generation circuitry 54) to generate a global clock signal (at the output of the circuit 54);

clock distribution circuitry 58 to distribute the global clock signal from the clock generation circuitry to a receiving point (the input terminal R of the PLL 72 in the circuit block 70A) at a second different location (because the circuits 54 and 72 are on different locations); and

a duty cycle correction circuit (the duty cycle correction circuit discussed in claim 1 above which is inside the block circuit 74) at the receiving point to correct the duty cycle of the distributed global clock signal.

As per claim 7, the recited other receiving point reads on the input terminal R of the PLL circuit 72 in the circuit block 70B, the limitation recited on the last two lines is met because the circuit block 70B also includes a duty cycle correction circuit in the circuit block 74.

As per claim 8, since the circuit 74 in the block circuit 70A includes a frequency multiplying circuit coupled to the duty cycle correction circuit as discussed in claim 4 above, the recited limitation is met.

As per claim 9, this claim is rejected for the same reason noted in claim 2.

As per claim 10, the recited signal reads on the signal on the feedback path discussed in claim 9 above which controls the variable delay element 110 as shown in Fig. 2.

As per claim 11, this claim is rejected for the same reason noted in claim 3.

As per claim 18, Markinson discloses an integrated circuit device (Fig. 1) comprising:

clock generation circuitry 54 for providing a first clock signal (at the output of the circuit 54) having a first duty cycle;

clock distribution network 58 coupled to the clock generation circuit 54 to distribute the first clock signal across the integrated circuit device; and

a plurality of duty cycle correction circuits (the circuits inside the block circuits 74 in the circuit blocks 70A and 70B) at receiving points (the points which receive the first clock signal distributed by the clock distribution network 58) to correct the duty cycle of the first clock signal at the receiving points.

As per claims 19-21, these claims are rejected for the same reasons noted in claims 8, 11 and 5, respectively.

As per claim 28, Markinson discloses a method (Fig. 1) comprising:

receiving an input clock signal (the circuit block 70A receives the input clock signal to an input terminal R of the circuit 72) from a clock distribution network 58 at an endpoint (the point

in the clock distribution network which outputs the signal to the input terminal R of the circuit 72) of the clock distribution network; and

correcting the duty cycle of the input clock signal (the circuit 74 in the circuit block 70A perform this function as discussed in claim 1) at the endpoint to provide a corrected output clock signal (the output signal to the bus interface circuit in the circuit block 70A).

As per claims 29-30, these claims are rejected for the same reasons noted in claims 9 and 11, respectively.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,398,262 to Ahuja discloses a clock distribution network (Fig. 2) which includes duty cycle correction circuit PLL 12, input buffer 11, a plurality of receiving buffers 21, ..., 30n.

US Patent No. 5,852,640 to Kliza et al discloses a clock distribution network (Fig. 5) which includes clock generation circuit 35, clock distribution network (the tree connection from the circuit 35 to the circuits 36-39, a plurality of duty cycle correction circuits 36-39 and a plurality of buffers 41-44.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MN
April 15, 2002

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800